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| Gerb-BMSTU_01 | **Министерство науки и высшего образования Российской Федерации**  **Федеральное государственное бюджетное образовательное учреждение**  **высшего образования**  **«Московский государственный технический университет**  **имени Н.Э. Баумана**  **(национальный исследовательский университет)»**  **(МГТУ им. Н.Э. Баумана)** |

ФАКУЛЬТЕТ **Информатика и системы управления**

КАФЕДРА **ПРОГРАММНОЕ ОБЕСПЕЧЕНИЕ ЭВМ И ИНФОРМАЦИОННЫЕ ТЕХНОЛОГИИ (ИУ7)**

НАПРАВЛЕНИЕ ПОДГОТОВКИ **09.03.04 Программная Инженерия**

**Отчет**

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| --- | --- |
| **по лабораторной работе №** | 4 |

**Название:**

Методологии разработки и верификации ускорителей вычислений на платформе XILINX ALVEO

**Дисциплина:** Архитектура ЭВМ

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Москва, 2021

# Введение

Цель работы – изучение архитектуры гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx.

В ходе лабораторной работы предлагается изучить основные сведения о платформе Xilinx Alveo U200, разработать RTL (Register Transfer Language, язык регистровых передач)) описание ускорителя вычислений по индивидуальному варианту, выполнить генерацию ядра ускорителя, выполнить синтез и сборку бинарного модуля ускорителя, разработать и отладить тестирующее программное обеспечение на серверной хост-платформе, провести тесты работы ускорителя вычислений.

Номер варианта: 14, функция ускорителя:

R[i] = A[i]/16 - 11 SLR1,DDR[1]

# Ход работы

На рисунке 1 представлена схема разрабатываемой аппаратной системы

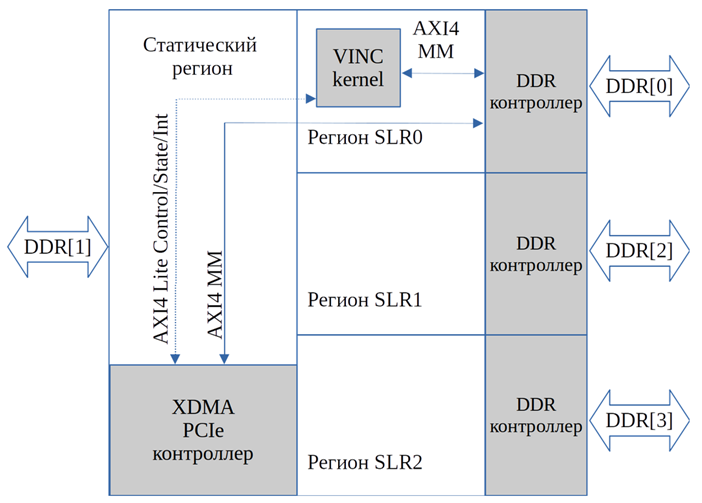


Рисунок 1. Функциональная схема аппаратной системы

Последовательность событий транзакции чтения можно представить следующим образом: ARVALID→ ARREADY→ RVALID→ RREADY.

На рисунке 2 представлена диаграмма чтения данных.



Рисунок 2. Транзакция чтения

Последовательность событий транзакции записи: AWVALID→ AWREADY → WVALID → WREADY → BVALID → BREADY.

На рисунке3 представлена диаграмма записи данных.

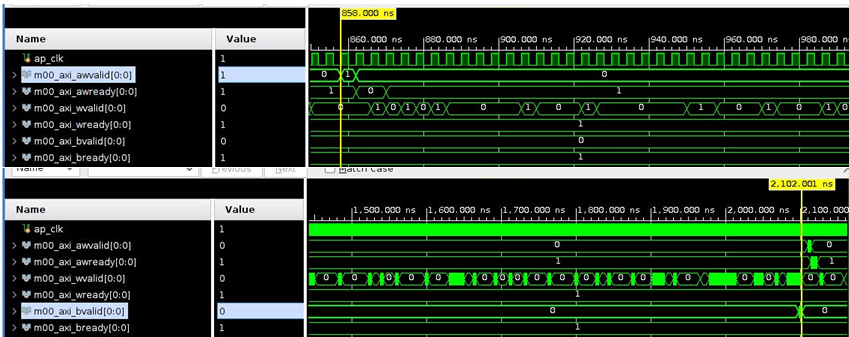


Рисунок 3. Транзакция записи

На рисунке 4 представлена диаграмма инкремента данных в модуле rtl\_kernel\_wizard\_0\_adder.v

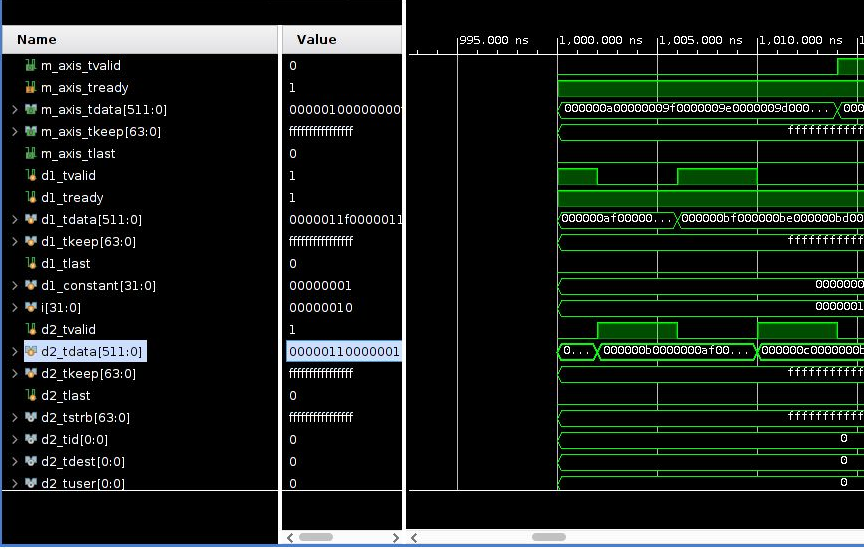


Рисунок 4. Диаграмма инкремента

На рисунке 5 представлено содержимое конфигурационного файла

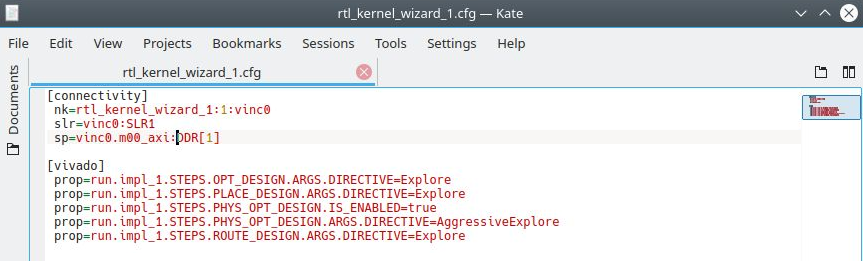


Рисунок 5. Конфигурационный файл

Путь к конфиг. файлу: /iu\_home/iu7134/workspace/ShatskiyR\_lab1/rtl\_kernel\_wizard\_1.cfg

Путь к .xo: /iu\_home/iu7134/workspace/ShatskiyR\_lab1\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_2\_ex/exports/rtl\_kernel\_wizard\_2.xo

Выходной файл: /iu\_home/iu7134/workspace/vinc.xclbin\_1

v++ -l -t hw -o /iu\_home/iu7134/workspace/vinc.xclbin\_1 -f xilinx\_u200\_xdma\_201830\_2 /iu\_home/iu7134/workspace/ShatskiyR\_lab1\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_2\_ex/exports/rtl\_kernel\_wizard\_2.xo --config /iu\_home/iu7134/workspace/ShatskiyR\_lab1/rtl\_kernel\_wizard\_1.cfg

**Содержимое файла v++\_vinc.log представлено ниже:**

INFO: [v++ 60-1306] Additional information associated with this v++ link can be found at:

Reports: /iu\_home/iu7134/\_x/reports/link

Log files: /iu\_home/iu7134/\_x/logs/link

INFO: [v++ 60-1548] Creating build summary session with primary output /iu\_home/iu7134/workspace/vinc.xclbin\_1.link\_summary, at Tue Dec 7 00:09:26 2021

INFO: [v++ 60-1316] Initiating connection to rulecheck server, at Tue Dec 7 00:09:26 2021

INFO: [v++ 60-1315] Creating rulecheck session with output '/iu\_home/iu7134/\_x/reports/link/v++\_link\_vinc\_guidance.html', at Tue Dec 7 00:09:45 2021

INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/xilinx\_u200\_xdma\_201830\_2/xilinx\_u200\_xdma\_201830\_2.xpfm

INFO: [v++ 60-1578] This platform contains Device Support Archive '/opt/xilinx/platforms/xilinx\_u200\_xdma\_201830\_2/hw/xilinx\_u200\_xdma\_201830\_2.dsa'

INFO: [v++ 74-74] Compiler Version string: 2020.2

INFO: [v++ 60-1302] Platform 'xilinx\_u200\_xdma\_201830\_2.xpfm' has been explicitly enabled for this release.

INFO: [v++ 60-629] Linking for hardware target

INFO: [v++ 60-423] Target device: xilinx\_u200\_xdma\_201830\_2

INFO: [v++ 60-1332] Run 'run\_link' status: Not started

INFO: [v++ 60-1443] [00:10:32] Run run\_link: Step system\_link: Started

INFO: [v++ 60-1453] Command Line: system\_link --xo /iu\_home/iu7134/workspace/ShatskiyR\_lab1\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_1\_ex/exports/rtl\_kernel\_wizard\_1.xo --config /iu\_home/iu7134/\_x/link/int/syslinkConfig.ini --xpfm /opt/xilinx/platforms/xilinx\_u200\_xdma\_201830\_2/xilinx\_u200\_xdma\_201830\_2.xpfm --target hw --output\_dir /iu\_home/iu7134/\_x/link/int --temp\_dir /iu\_home/iu7134/\_x/link/sys\_link

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7134/\_x/link/run\_link

INFO: [SYSTEM\_LINK 60-1316] Initiating connection to rulecheck server, at Tue Dec 7 00:10:43 2021

INFO: [SYSTEM\_LINK 82-70] Extracting xo v3 file /iu\_home/iu7134/workspace/ShatskiyR\_lab1\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_1\_ex/exports/rtl\_kernel\_wizard\_1.xo

INFO: [SYSTEM\_LINK 82-53] Creating IP database /iu\_home/iu7134/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-38] [00:10:45] build\_xd\_ip\_db started: /data/Xilinx/Vitis/2020.2/bin/build\_xd\_ip\_db -ip\_search 0 -sds-pf /iu\_home/iu7134/\_x/link/sys\_link/xilinx\_u200\_xdma\_201830\_2.hpfm -clkid 0 -ip /iu\_home/iu7134/\_x/link/sys\_link/iprepo/mycompany\_com\_kernel\_rtl\_kernel\_wizard\_1\_1\_0,rtl\_kernel\_wizard\_1 -o /iu\_home/iu7134/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-37] [00:11:16] build\_xd\_ip\_db finished successfully

Time (s): cpu = 00:00:31 ; elapsed = 00:00:30 . Memory (MB): peak = 1557.891 ; gain = 0.000 ; free physical = 73951 ; free virtual = 243909

INFO: [SYSTEM\_LINK 82-51] Create system connectivity graph

INFO: [SYSTEM\_LINK 82-102] Applying explicit connections to the system connectivity graph: /iu\_home/iu7134/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [SYSTEM\_LINK 82-38] [00:11:16] cfgen started: /data/Xilinx/Vitis/2020.2/bin/cfgen -nk rtl\_kernel\_wizard\_1:1:vinc0 -slr vinc0:SLR1 -sp vinc0.m00\_axi:DDR[1] -dmclkid 0 -r /iu\_home/iu7134/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o /iu\_home/iu7134/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [CFGEN 83-0] Kernel Specs:

INFO: [CFGEN 83-0] kernel: rtl\_kernel\_wizard\_1, num: 1 {vinc0}

INFO: [CFGEN 83-0] Port Specs:

INFO: [CFGEN 83-0] kernel: vinc0, k\_port: m00\_axi, sptag: DDR[1]

INFO: [CFGEN 83-0] SLR Specs:

INFO: [CFGEN 83-0] instance: vinc0, SLR: SLR1

INFO: [CFGEN 83-2228] Creating mapping for argument vinc0.axi00\_ptr0 to DDR[1] for directive vinc0.m00\_axi:DDR[1]

INFO: [SYSTEM\_LINK 82-37] [00:11:42] cfgen finished successfully

Time (s): cpu = 00:00:25 ; elapsed = 00:00:26 . Memory (MB): peak = 1557.891 ; gain = 0.000 ; free physical = 73431 ; free virtual = 243399

INFO: [SYSTEM\_LINK 82-52] Create top-level block diagram

INFO: [SYSTEM\_LINK 82-38] [00:11:42] cf2bd started: /data/Xilinx/Vitis/2020.2/bin/cf2bd --linux --trace\_buffer 1024 --input\_file /iu\_home/iu7134/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml --ip\_db /iu\_home/iu7134/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml --cf\_name dr --working\_dir /iu\_home/iu7134/\_x/link/sys\_link/\_sysl/.xsd --temp\_dir /iu\_home/iu7134/\_x/link/sys\_link --output\_dir /iu\_home/iu7134/\_x/link/int --target\_bd pfm\_dynamic.bd

INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer 1024 -i /iu\_home/iu7134/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml -r /iu\_home/iu7134/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o dr.xml

INFO: [CF2BD 82-28] cf2xd finished successfully

INFO: [CF2BD 82-31] Launching cf\_xsd: cf\_xsd -disable-address-gen -bd pfm\_dynamic.bd -dn dr -dp /iu\_home/iu7134/\_x/link/sys\_link/\_sysl/.xsd

INFO: [CF2BD 82-28] cf\_xsd finished successfully

INFO: [SYSTEM\_LINK 82-37] [00:11:56] cf2bd finished successfully

Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1557.891 ; gain = 0.000 ; free physical = 73244 ; free virtual = 243314

INFO: [v++ 60-1441] [00:11:56] Run run\_link: Step system\_link: Completed

Time (s): cpu = 00:01:21 ; elapsed = 00:01:24 . Memory (MB): peak = 1576.969 ; gain = 0.000 ; free physical = 73282 ; free virtual = 243347

INFO: [v++ 60-1443] [00:11:56] Run run\_link: Step cf2sw: Started

INFO: [v++ 60-1453] Command Line: cf2sw -sdsl /iu\_home/iu7134/\_x/link/int/sdsl.dat -rtd /iu\_home/iu7134/\_x/link/int/cf2sw.rtd -nofilter /iu\_home/iu7134/\_x/link/int/cf2sw\_full.rtd -xclbin /iu\_home/iu7134/\_x/link/int/xclbin\_orig.xml -o /iu\_home/iu7134/\_x/link/int/xclbin\_orig.1.xml

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7134/\_x/link/run\_link

INFO: [v++ 60-1441] [00:12:11] Run run\_link: Step cf2sw: Completed

Time (s): cpu = 00:00:14 ; elapsed = 00:00:15 . Memory (MB): peak = 1576.969 ; gain = 0.000 ; free physical = 72433 ; free virtual = 242483

INFO: [v++ 60-1443] [00:12:11] Run run\_link: Step rtd2\_system\_diagram: Started

INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7134/\_x/link/run\_link

INFO: [v++ 60-1441] [00:12:21] Run run\_link: Step rtd2\_system\_diagram: Completed

Time (s): cpu = 00:00:00 ; elapsed = 00:00:10 . Memory (MB): peak = 1576.969 ; gain = 0.000 ; free physical = 71874 ; free virtual = 241925

INFO: [v++ 60-1443] [00:12:21] Run run\_link: Step vpl: Started

INFO: [v++ 60-1453] Command Line: vpl -t hw -f xilinx\_u200\_xdma\_201830\_2 --remote\_ip\_cache /iu\_home/iu7134/.ipcache --output\_dir /iu\_home/iu7134/\_x/link/int --log\_dir /iu\_home/iu7134/\_x/logs/link --report\_dir /iu\_home/iu7134/\_x/reports/link --config /iu\_home/iu7134/\_x/link/int/vplConfig.ini -k /iu\_home/iu7134/\_x/link/int/kernel\_info.dat --webtalk\_flag Vitis --temp\_dir /iu\_home/iu7134/\_x/link --no-info --iprepo /iu\_home/iu7134/\_x/link/int/xo/ip\_repo/mycompany\_com\_kernel\_rtl\_kernel\_wizard\_1\_1\_0 --messageDb /iu\_home/iu7134/\_x/link/run\_link/vpl.pb /iu\_home/iu7134/\_x/link/int/dr.bd.tcl

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7134/\_x/link/run\_link

\*\*\*\*\*\* vpl v2020.2 (64-bit)

\*\*\*\* SW Build (by xbuild) on 2020-11-18-05:13:29

\*\* Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

INFO: [VPL 60-839] Read in kernel information from file '/iu\_home/iu7134/\_x/link/int/kernel\_info.dat'.

INFO: [VPL 74-74] Compiler Version string: 2020.2

INFO: [VPL 60-423] Target device: xilinx\_u200\_xdma\_201830\_2

INFO: [VPL 60-1032] Extracting hardware platform to /iu\_home/iu7134/\_x/link/vivado/vpl/.local/hw\_platform

WARNING: /data/Xilinx/Vitis/2020.2/tps/lnx64/jre9.0.4 does not exist.

[00:17:46] Run vpl: Step create\_project: RUNNING...

[00:17:38] Run vpl: Step create\_project: Started

Creating Vivado project.

[00:18:07] Run vpl: Step create\_project: Completed

[00:18:07] Run vpl: Step create\_bd: Started

[00:19:51] Run vpl: Step create\_bd: RUNNING...

[00:21:25] Run vpl: Step create\_bd: RUNNING...

[00:22:55] Run vpl: Step create\_bd: RUNNING...

[00:24:46] Run vpl: Step create\_bd: RUNNING...

[00:26:18] Run vpl: Step create\_bd: RUNNING...

[00:27:14] Run vpl: Step create\_bd: Completed

[00:27:14] Run vpl: Step update\_bd: Started

[00:27:17] Run vpl: Step update\_bd: Completed

[00:27:17] Run vpl: Step generate\_target: Started

[00:28:50] Run vpl: Step generate\_target: RUNNING...

[00:30:25] Run vpl: Step generate\_target: RUNNING...

[00:31:58] Run vpl: Step generate\_target: RUNNING...

[00:33:40] Run vpl: Step generate\_target: RUNNING...

[00:35:22] Run vpl: Step generate\_target: RUNNING...

[00:36:13] Run vpl: Step generate\_target: Completed

[00:36:13] Run vpl: Step config\_hw\_runs: Started

[00:36:26] Run vpl: Step config\_hw\_runs: Completed

[00:36:26] Run vpl: Step synth: Started

[00:38:26] Top-level synthesis in progress.

[00:39:03] Top-level synthesis in progress.

[00:39:40] Top-level synthesis in progress.

[00:40:16] Top-level synthesis in progress.

[00:40:56] Top-level synthesis in progress.

[00:41:36] Top-level synthesis in progress.

[00:42:14] Top-level synthesis in progress.

[00:42:57] Top-level synthesis in progress.

[00:43:36] Top-level synthesis in progress.

[00:44:16] Top-level synthesis in progress.

[00:44:55] Top-level synthesis in progress.

[00:45:37] Top-level synthesis in progress.

[00:46:15] Top-level synthesis in progress.

[00:46:53] Top-level synthesis in progress.

[00:47:31] Top-level synthesis in progress.

[00:48:12] Top-level synthesis in progress.

[00:49:02] Run vpl: Step synth: Completed

[00:49:02] Run vpl: Step impl: Started

[01:44:34] Finished 2nd of 6 tasks (FPGA linking synthesized kernels to platform). Elapsed time: 01h 32m 02s

[01:44:34] Starting logic optimization..

[01:53:17] Phase 1 Retarget

[01:55:09] Phase 2 Constant propagation

[01:57:07] Phase 3 Sweep

[02:01:24] Phase 4 BUFG optimization

[02:02:37] Phase 5 Shift Register Optimization

[02:03:13] Phase 6 Post Processing Netlist

[02:16:52] Finished 3rd of 6 tasks (FPGA logic optimization). Elapsed time: 00h 32m 17s

[02:16:52] Starting logic placement..

[02:21:15] Phase 1 Placer Initialization

[02:21:15] Phase 1.1 Placer Initialization Netlist Sorting

[02:35:03] Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

[02:43:26] Phase 1.3 Build Placer Netlist Model

[02:55:25] Phase 1.4 Constrain Clocks/Macros

[02:56:45] Phase 2 Global Placement

[02:56:45] Phase 2.1 Floorplanning

[02:59:52] Phase 2.1.1 Partition Driven Placement

[02:59:52] Phase 2.1.1.1 PBP: Partition Driven Placement

[03:01:07] Phase 2.1.1.2 PBP: Clock Region Placement

[03:04:57] Phase 2.1.1.3 PBP: Compute Congestion

[03:05:34] Phase 2.1.1.4 PBP: UpdateTiming

[03:07:26] Phase 2.1.1.5 PBP: Add part constraints

[03:08:03] Phase 2.2 Update Timing before SLR Path Opt

[03:08:41] Phase 2.3 Global Placement Core

[03:31:51] Phase 2.3.1 Physical Synthesis In Placer

[03:41:50] Phase 3 Detail Placement

[03:41:50] Phase 3.1 Commit Multi Column Macros

[03:42:28] Phase 3.2 Commit Most Macros & LUTRAMs

[03:47:31] Phase 3.3 Small Shape DP

[03:47:31] Phase 3.3.1 Small Shape Clustering

[03:49:32] Phase 3.3.2 Flow Legalize Slice Clusters

[03:49:32] Phase 3.3.3 Slice Area Swap

[03:54:06] Phase 3.4 Place Remaining

[03:54:06] Phase 3.5 Re-assign LUT pins

[03:55:23] Phase 3.6 Pipeline Register Optimization

[03:55:23] Phase 3.7 Fast Optimization

[03:59:43] Phase 4 Post Placement Optimization and Clean-Up

[03:59:43] Phase 4.1 Post Commit Optimization

[04:08:03] Phase 4.1.1 Post Placement Optimization

[04:08:40] Phase 4.1.1.1 BUFG Insertion

[04:08:40] Phase 1 Physical Synthesis Initialization

[04:11:12] Phase 4.1.1.2 BUFG Replication

[04:13:08] Phase 4.1.1.3 Replication

[04:18:56] Phase 4.2 Post Placement Cleanup

[04:19:34] Phase 4.3 Placer Reporting

[04:19:34] Phase 4.3.1 Print Estimated Congestion

[04:21:30] Phase 4.4 Final Placement Cleanup

[05:26:24] Finished 4th of 6 tasks (FPGA logic placement). Elapsed time: 03h 09m 32s

[05:26:24] Starting logic routing..

[05:31:23] Phase 1 Build RT Design

[05:40:53] Phase 2 Router Initialization

[05:40:53] Phase 2.1 Fix Topology Constraints

[05:41:29] Phase 2.2 Pre Route Cleanup

[05:42:06] Phase 2.3 Global Clock Net Routing

[05:43:58] Phase 2.4 Update Timing

[05:55:59] Phase 2.5 Update Timing for Bus Skew

[05:55:59] Phase 2.5.1 Update Timing

[06:00:21] Phase 3 Initial Routing

[06:00:21] Phase 3.1 Global Routing

[06:04:48] Phase 4 Rip-up And Reroute

[06:04:48] Phase 4.1 Global Iteration 0

[06:23:32] Phase 4.2 Global Iteration 1

[06:33:51] Phase 5 Delay and Skew Optimization

[06:33:51] Phase 5.1 Delay CleanUp

[06:33:51] Phase 5.1.1 Update Timing

[06:40:19] Phase 5.2 Clock Skew Optimization

[06:40:57] Phase 6 Post Hold Fix

[06:40:57] Phase 6.1 Hold Fix Iter

[06:40:57] Phase 6.1.1 Update Timing

[06:45:19] Phase 7 Route finalize

[06:45:57] Phase 8 Verifying routed nets

[06:47:11] Phase 9 Depositing Routes

[06:51:02] Phase 10 Route finalize

[06:51:02] Phase 11 Post Router Timing

[06:57:17] Finished 5th of 6 tasks (FPGA routing). Elapsed time: 01h 30m 52s

[06:57:17] Starting bitstream generation..

[08:49:26] Creating bitmap...

[09:36:16] Writing bitstream ./pfm\_top\_i\_dynamic\_region\_my\_rm\_partial.bit...

[09:36:54] Finished 6th of 6 tasks (FPGA bitstream generation). Elapsed time: 02h 39m 37s

[09:39:53] Run vpl: Step impl: Completed

[09:40:01] Run vpl: FINISHED. Run Status: impl Complete!

INFO: [v++ 60-1441] [09:40:24] Run run\_link: Step vpl: Completed

Time (s): cpu = 00:16:56 ; elapsed = 09:28:03 . Memory (MB): peak = 1576.969 ; gain = 0.000 ; free physical = 113718 ; free virtual = 278521

INFO: [v++ 60-1443] [09:40:24] Run run\_link: Step rtdgen: Started

INFO: [v++ 60-1453] Command Line: rtdgen

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7134/\_x/link/run\_link

INFO: [v++ 60-991] clock name 'clkwiz\_kernel\_clk\_out1' (clock ID '0') is being mapped to clock name 'DATA\_CLK' in the xclbin

INFO: [v++ 60-991] clock name 'clkwiz\_kernel2\_clk\_out1' (clock ID '1') is being mapped to clock name 'KERNEL\_CLK' in the xclbin

INFO: [v++ 60-1230] The compiler selected the following frequencies for the runtime controllable kernel clock(s) and scalable system clock(s): Kernel (DATA) clock: clkwiz\_kernel\_clk\_out1 = 300, Kernel (KERNEL) clock: clkwiz\_kernel2\_clk\_out1 = 500

INFO: [v++ 60-1453] Command Line: cf2sw -a /iu\_home/iu7134/\_x/link/int/address\_map.xml -sdsl /iu\_home/iu7134/\_x/link/int/sdsl.dat -xclbin /iu\_home/iu7134/\_x/link/int/xclbin\_orig.xml -rtd /iu\_home/iu7134/\_x/link/int/vinc.rtd -o /iu\_home/iu7134/\_x/link/int/vinc.xml

INFO: [v++ 60-1652] Cf2sw returned exit code: 0

INFO: [v++ 60-2311] HPISystemDiagram::writeSystemDiagramAfterRunningVivado, rtdInputFilePath: /iu\_home/iu7134/\_x/link/int/vinc.rtd

INFO: [v++ 60-2312] HPISystemDiagram::writeSystemDiagramAfterRunningVivado, systemDiagramOutputFilePath: /iu\_home/iu7134/\_x/link/int/systemDiagramModelSlrBaseAddress.json

INFO: [v++ 60-1618] Launching

INFO: [v++ 60-1441] [09:40:38] Run run\_link: Step rtdgen: Completed

Time (s): cpu = 00:00:13 ; elapsed = 00:00:14 . Memory (MB): peak = 1576.969 ; gain = 0.000 ; free physical = 113641 ; free virtual = 278504

INFO: [v++ 60-1443] [09:40:38] Run run\_link: Step xclbinutil: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --add-section DEBUG\_IP\_LAYOUT:JSON:/iu\_home/iu7134/\_x/link/int/debug\_ip\_layout.rtd --add-section BITSTREAM:RAW:/iu\_home/iu7134/\_x/link/int/partial.bit --force --target hw --key-value SYS:dfx\_enable:true --add-section :JSON:/iu\_home/iu7134/\_x/link/int/vinc.rtd --append-section :JSON:/iu\_home/iu7134/\_x/link/int/appendSection.rtd --add-section CLOCK\_FREQ\_TOPOLOGY:JSON:/iu\_home/iu7134/\_x/link/int/vinc\_xml.rtd --add-section BUILD\_METADATA:JSON:/iu\_home/iu7134/\_x/link/int/vinc\_build.rtd --add-section EMBEDDED\_METADATA:RAW:/iu\_home/iu7134/\_x/link/int/vinc.xml --add-section SYSTEM\_METADATA:RAW:/iu\_home/iu7134/\_x/link/int/systemDiagramModelSlrBaseAddress.json --output /iu\_home/iu7134/workspace/vinc.xclbin\_1

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7134/\_x/link/run\_link

XRT Build Version: 2.8.743 (2020.2)

Build Date: 2020-11-16 00:19:11

Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9

Creating a default 'in-memory' xclbin image.

Section: 'DEBUG\_IP\_LAYOUT'(9) was successfully added.

Size : 440 bytes

Format : JSON

File : '/iu\_home/iu7134/\_x/link/int/debug\_ip\_layout.rtd'

Section: 'BITSTREAM'(0) was successfully added.

Size : 39912114 bytes

Format : RAW

File : '/iu\_home/iu7134/\_x/link/int/partial.bit'

Section: 'MEM\_TOPOLOGY'(6) was successfully added.

Format : JSON

File : 'mem\_topology'

Section: 'IP\_LAYOUT'(8) was successfully added.

Format : JSON

File : 'ip\_layout'

Section: 'CONNECTIVITY'(7) was successfully added.

Format : JSON

File : 'connectivity'

Section: 'CLOCK\_FREQ\_TOPOLOGY'(11) was successfully added.

Size : 274 bytes

Format : JSON

File : '/iu\_home/iu7134/\_x/link/int/vinc\_xml.rtd'

Section: 'BUILD\_METADATA'(14) was successfully added.

Size : 3089 bytes

Format : JSON

File : '/iu\_home/iu7134/\_x/link/int/vinc\_build.rtd'

Section: 'EMBEDDED\_METADATA'(2) was successfully added.

Size : 2759 bytes

Format : RAW

File : '/iu\_home/iu7134/\_x/link/int/vinc.xml'

Section: 'SYSTEM\_METADATA'(22) was successfully added.

Size : 5793 bytes

Format : RAW

File : '/iu\_home/iu7134/\_x/link/int/systemDiagramModelSlrBaseAddress.json'

Section: 'IP\_LAYOUT'(8) was successfully appended to.

Format : JSON

File : 'ip\_layout'

Successfully wrote (39934570 bytes) to the output file: /iu\_home/iu7134/workspace/vinc.xclbin\_1

Leaving xclbinutil.

INFO: [v++ 60-1441] [09:40:40] Run run\_link: Step xclbinutil: Completed

Time (s): cpu = 00:00:00.46 ; elapsed = 00:00:02 . Memory (MB): peak = 1576.969 ; gain = 0.000 ; free physical = 113575 ; free virtual = 278515

INFO: [v++ 60-1443] [09:40:40] Run run\_link: Step xclbinutilinfo: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info /iu\_home/iu7134/workspace/vinc.xclbin.info --input /iu\_home/iu7134/workspace/vinc.xclbin\_1

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7134/\_x/link/run\_link

INFO: [v++ 60-1441] [09:40:43] Run run\_link: Step xclbinutilinfo: Completed

Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1576.969 ; gain = 0.000 ; free physical = 113543 ; free virtual = 278482

INFO: [v++ 60-1443] [09:40:43] Run run\_link: Step generate\_sc\_driver: Started

INFO: [v++ 60-1453] Command Line:

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7134/\_x/link/run\_link

INFO: [v++ 60-1441] [09:40:43] Run run\_link: Step generate\_sc\_driver: Completed

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.05 . Memory (MB): peak = 1576.969 ; gain = 0.000 ; free physical = 113545 ; free virtual = 278484

INFO: [v++ 60-244] Generating system estimate report...

INFO: [v++ 60-1092] Generated system estimate report: /iu\_home/iu7134/\_x/reports/link/system\_estimate\_vinc.xtxt

INFO: [v++ 60-586] Created /iu\_home/iu7134/workspace/vinc.ltx

INFO: [v++ 60-586] Created /iu\_home/iu7134/workspace/vinc.xclbin\_1

INFO: [v++ 60-1307] Run completed. Additional information can be found in:

Guidance: /iu\_home/iu7134/\_x/reports/link/v++\_link\_vinc\_guidance.html

Timing Report: /iu\_home/iu7134/\_x/reports/link/imp/impl\_1\_xilinx\_u200\_xdma\_201830\_2\_bb\_locked\_timing\_summary\_routed.rpt

Vivado Log: /iu\_home/iu7134/\_x/logs/link/vivado.log

Steps Log File: /iu\_home/iu7134/\_x/logs/link/link.steps.log

INFO: [v++ 60-2343] Use the vitis\_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis\_analyzer /iu\_home/iu7134/workspace/vinc.xclbin\_1.link\_summary

INFO: [v++ 60-791] Total elapsed time: 9h 32m 7s

INFO: [v++ 60-1653] Closing dispatch client.

**Содержимое файла vinc.xclbin.info приведено ниже:**

==============================================================================

XRT Build Version: 2.8.743 (2020.2)

Build Date: 2020-11-16 00:19:11

Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9

==============================================================================

xclbin Information

------------------

Generated by: v++ (2020.2) on 2020-11-18-05:13:29

Version: 2.8.743

Kernels: rtl\_kernel\_wizard\_1

Signature:

Content: Bitstream

UUID (xclbin): f3f63637-0591-4499-be99-4754be03ad0e

Sections: DEBUG\_IP\_LAYOUT, BITSTREAM, MEM\_TOPOLOGY, IP\_LAYOUT,

CONNECTIVITY, CLOCK\_FREQ\_TOPOLOGY, BUILD\_METADATA,

EMBEDDED\_METADATA, SYSTEM\_METADATA,

GROUP\_CONNECTIVITY, GROUP\_TOPOLOGY

==============================================================================

Hardware Platform (Shell) Information

-------------------------------------

Vendor: xilinx

Board: u200

Name: xdma

Version: 201830.2

Generated Version: Vivado 2018.3 (SW Build: 2568420)

Created: Tue Jun 25 06:55:20 2019

FPGA Device: xcu200

Board Vendor: xilinx.com

Board Name: xilinx.com:au200:1.0

Board Part: xilinx.com:au200:part0:1.0

Platform VBNV: xilinx\_u200\_xdma\_201830\_2

Static UUID: c102e7af-b2b8-4381-992b-9a00cc3863eb

Feature ROM TimeStamp: 1561465320

Clocks

------

Name: DATA\_CLK

Index: 0

Type: DATA

Frequency: 300 MHz

Name: KERNEL\_CLK

Index: 1

Type: KERNEL

Frequency: 500 MHz

Memory Configuration

--------------------

Name: bank0

Index: 0

Type: MEM\_DDR4

Base Address: 0x4000000000

Address Size: 0x400000000

Bank Used: No

Name: bank1

Index: 1

Type: MEM\_DDR4

Base Address: 0x5000000000

Address Size: 0x400000000

Bank Used: Yes

Name: bank2

Index: 2

Type: MEM\_DDR4

Base Address: 0x6000000000

Address Size: 0x400000000

Bank Used: No

Name: bank3

Index: 3

Type: MEM\_DDR4

Base Address: 0x7000000000

Address Size: 0x400000000

Bank Used: No

Name: PLRAM[0]

Index: 4

Type: MEM\_DRAM

Base Address: 0x3000000000

Address Size: 0x20000

Bank Used: No

Name: PLRAM[1]

Index: 5

Type: MEM\_DRAM

Base Address: 0x3000200000

Address Size: 0x20000

Bank Used: No

Name: PLRAM[2]

Index: 6

Type: MEM\_DRAM

Base Address: 0x3000400000

Address Size: 0x20000

Bank Used: No

==============================================================================

Kernel: rtl\_kernel\_wizard\_1

Definition

----------

Signature: rtl\_kernel\_wizard\_1 (uint scalar00, int\* axi00\_ptr0)

Ports

-----

Port: s\_axi\_control

Mode: slave

Range (bytes): 0x1000

Data Width: 32 bits

Port Type: addressable

Port: m00\_axi

Mode: master

Range (bytes): 0xFFFFFFFFFFFFFFFF

Data Width: 512 bits

Port Type: addressable

--------------------------

Instance: vinc0

Base Address: 0x1800000

Argument: scalar00

Register Offset: 0x010

Port: s\_axi\_control

Memory: <not applicable>

Argument: axi00\_ptr0

Register Offset: 0x018

Port: m00\_axi

Memory: bank1 (MEM\_DDR4)

==============================================================================

Generated By

------------

Command: v++

Version: 2020.2 - 2020-11-18-05:13:29 (SW BUILD: 0)

Command Line: v++ --config /iu\_home/iu7134/workspace/ShatskiyR\_lab1/rtl\_kernel\_wizard\_1.cfg --connectivity.nk rtl\_kernel\_wizard\_1:1:vinc0 --connectivity.slr vinc0:SLR1 --connectivity.sp vinc0.m00\_axi:DDR[1] --input\_files /iu\_home/iu7134/workspace/ShatskiyR\_lab1\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_1\_ex/exports/rtl\_kernel\_wizard\_1.xo --link --optimize 0 --output /iu\_home/iu7134/workspace/vinc.xclbin\_1 --platform xilinx\_u200\_xdma\_201830\_2 --report\_level 0 --target hw --vivado.prop run.impl\_1.STEPS.OPT\_DESIGN.ARGS.DIRECTIVE=Explore --vivado.prop run.impl\_1.STEPS.PLACE\_DESIGN.ARGS.DIRECTIVE=Explore --vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.IS\_ENABLED=true --vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.ARGS.DIRECTIVE=AggressiveExplore --vivado.prop run.impl\_1.STEPS.ROUTE\_DESIGN.ARGS.DIRECTIVE=Explore

Options: --config /iu\_home/iu7134/workspace/ShatskiyR\_lab1/rtl\_kernel\_wizard\_1.cfg

--connectivity.nk rtl\_kernel\_wizard\_1:1:vinc0

--connectivity.slr vinc0:SLR1

--connectivity.sp vinc0.m00\_axi:DDR[1]

--input\_files /iu\_home/iu7134/workspace/ShatskiyR\_lab1\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_1\_ex/exports/rtl\_kernel\_wizard\_1.xo

--link

--optimize 0

--output /iu\_home/iu7134/workspace/vinc.xclbin\_1

--platform xilinx\_u200\_xdma\_201830\_2

--report\_level 0

--target hw

--vivado.prop run.impl\_1.STEPS.OPT\_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl\_1.STEPS.PLACE\_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.IS\_ENABLED=true

--vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.ARGS.DIRECTIVE=AggressiveExplore

--vivado.prop run.impl\_1.STEPS.ROUTE\_DESIGN.ARGS.DIRECTIVE=Explore

==============================================================================

User Added Key Value Pairs

--------------------------

<empty>

# Индивидуальное задание

Функция ядра: R[i] = A[i]/16 – 11, регион: SLR1,DDR[1].

Ниже приведен измененный код ядра:

// This is a generated file. Use and modify at your own risk.

////////////////////////////////////////////////////////////////////////////////

// Description: Pipelined adder. This is an adder with pipelines before and

// after the adder datapath. The output is fed into a FIFO and prog\_full is

// used to signal ready. This design allows for high Fmax.

// default\_nettype of none prevents implicit wire declaration.

`default\_nettype none

`timescale 1ps / 1ps

module rtl\_kernel\_wizard\_1\_example\_adder #(

parameter integer C\_AXIS\_TDATA\_WIDTH = 512, // Data width of both input and output data

parameter integer C\_ADDER\_BIT\_WIDTH = 32,

parameter integer C\_NUM\_CLOCKS = 1

)

(

input wire [C\_ADDER\_BIT\_WIDTH-1:0] ctrl\_constant,

input wire s\_axis\_aclk,

input wire s\_axis\_areset,

input wire s\_axis\_tvalid,

output wire s\_axis\_tready,

input wire [C\_AXIS\_TDATA\_WIDTH-1:0] s\_axis\_tdata,

input wire [C\_AXIS\_TDATA\_WIDTH/8-1:0] s\_axis\_tkeep,

input wire s\_axis\_tlast,

input wire m\_axis\_aclk,

output wire m\_axis\_tvalid,

input wire m\_axis\_tready,

output wire [C\_AXIS\_TDATA\_WIDTH-1:0] m\_axis\_tdata,

output wire [C\_AXIS\_TDATA\_WIDTH/8-1:0] m\_axis\_tkeep,

output wire m\_axis\_tlast

);

localparam integer LP\_NUM\_LOOPS = C\_AXIS\_TDATA\_WIDTH/C\_ADDER\_BIT\_WIDTH;

localparam LP\_CLOCKING\_MODE = C\_NUM\_CLOCKS == 1 ? "common\_clock" : "independent\_clock";

/////////////////////////////////////////////////////////////////////////////

// Variables

/////////////////////////////////////////////////////////////////////////////

reg d1\_tvalid = 1'b0;

reg d1\_tready = 1'b0;

reg [C\_AXIS\_TDATA\_WIDTH-1:0] d1\_tdata;

reg [C\_AXIS\_TDATA\_WIDTH/8-1:0] d1\_tkeep;

reg d1\_tlast;

reg [C\_ADDER\_BIT\_WIDTH-1:0] d1\_constant;

integer i;

reg d2\_tvalid = 1'b0;

reg [C\_AXIS\_TDATA\_WIDTH-1:0] d2\_tdata;

reg [C\_AXIS\_TDATA\_WIDTH/8-1:0] d2\_tkeep;

reg d2\_tlast;

wire [C\_AXIS\_TDATA\_WIDTH/8-1:0] d2\_tstrb;

wire [0:0] d2\_tid;

wire [0:0] d2\_tdest;

wire [0:0] d2\_tuser;

wire prog\_full\_axis;

reg fifo\_ready\_r = 1'b0;

/////////////////////////////////////////////////////////////////////////////

// RTL Logic

/////////////////////////////////////////////////////////////////////////////

// Register s\_axis\_interface/inputs

always @(posedge s\_axis\_aclk) begin

d1\_tvalid <= s\_axis\_tvalid;

d1\_tready <= s\_axis\_tready;

d1\_tdata <= s\_axis\_tdata;

d1\_tkeep <= s\_axis\_tkeep;

d1\_tlast <= s\_axis\_tlast;

d1\_constant <= ctrl\_constant;

end

// Adder function

always @(posedge s\_axis\_aclk) begin

for (i = 0; i < LP\_NUM\_LOOPS; i = i + 1) begin

**d2\_tdata[i\*C\_ADDER\_BIT\_WIDTH+:C\_ADDER\_BIT\_WIDTH] <= d1\_tdata[C\_ADDER\_BIT\_WIDTH\*i+:C\_ADDER\_BIT\_WIDTH] / 16 - 11;**

end

end

// Register inputs to fifo

always @(posedge s\_axis\_aclk) begin

d2\_tvalid <= d1\_tvalid & d1\_tready;

d2\_tkeep <= d1\_tkeep;

d2\_tlast <= d1\_tlast;

end

// Tie-off unused inputs to FIFO.

assign d2\_tstrb = {C\_AXIS\_TDATA\_WIDTH/8{1'b1}};

assign d2\_tid = 1'b0;

assign d2\_tdest = 1'b0;

assign d2\_tuser = 1'b0;

always @(posedge s\_axis\_aclk) begin

fifo\_ready\_r <= ~prog\_full\_axis;

end

assign s\_axis\_tready = fifo\_ready\_r;

xpm\_fifo\_axis #(

.CDC\_SYNC\_STAGES ( 2 ) , // DECIMAL

.CLOCKING\_MODE ( LP\_CLOCKING\_MODE ) , // String

.ECC\_MODE ( "no\_ecc" ) , // String

.FIFO\_DEPTH ( 32 ) , // DECIMAL

.FIFO\_MEMORY\_TYPE ( "distributed" ) , // String

.PACKET\_FIFO ( "false" ) , // String

.PROG\_EMPTY\_THRESH ( 5 ) , // DECIMAL

.PROG\_FULL\_THRESH ( 32-5 ) , // DECIMAL

.RD\_DATA\_COUNT\_WIDTH ( 6 ) , // DECIMAL

.RELATED\_CLOCKS ( 0 ) , // DECIMAL

.TDATA\_WIDTH ( C\_AXIS\_TDATA\_WIDTH ) , // DECIMAL

.TDEST\_WIDTH ( 1 ) , // DECIMAL

.TID\_WIDTH ( 1 ) , // DECIMAL

.TUSER\_WIDTH ( 1 ) , // DECIMAL

.USE\_ADV\_FEATURES ( "1002" ) , // String: Only use prog\_full

.WR\_DATA\_COUNT\_WIDTH ( 6 ) // DECIMAL

)

inst\_xpm\_fifo\_axis (

.s\_aclk ( s\_axis\_aclk ) ,

.s\_aresetn ( ~s\_axis\_areset ) ,

.s\_axis\_tvalid ( d2\_tvalid ) ,

.s\_axis\_tready ( ) ,

.s\_axis\_tdata ( d2\_tdata ) ,

.s\_axis\_tstrb ( d2\_tstrb ) ,

.s\_axis\_tkeep ( d2\_tkeep ) ,

.s\_axis\_tlast ( d2\_tlast ) ,

.s\_axis\_tid ( d2\_tid ) ,

.s\_axis\_tdest ( d2\_tdest ) ,

.s\_axis\_tuser ( d2\_tuser ) ,

.almost\_full\_axis ( ) ,

.prog\_full\_axis ( prog\_full\_axis ) ,

.wr\_data\_count\_axis ( ) ,

.injectdbiterr\_axis ( 1'b0 ) ,

.injectsbiterr\_axis ( 1'b0 ) ,

.m\_aclk ( m\_axis\_aclk ) ,

.m\_axis\_tvalid ( m\_axis\_tvalid ) ,

.m\_axis\_tready ( m\_axis\_tready ) ,

.m\_axis\_tdata ( m\_axis\_tdata ) ,

.m\_axis\_tstrb ( ) ,

.m\_axis\_tkeep ( m\_axis\_tkeep ) ,

.m\_axis\_tlast ( m\_axis\_tlast ) ,

.m\_axis\_tid ( ) ,

.m\_axis\_tdest ( ) ,

.m\_axis\_tuser ( ) ,

.almost\_empty\_axis ( ) ,

.prog\_empty\_axis ( ) ,

.rd\_data\_count\_axis ( ) ,

.sbiterr\_axis ( ) ,

.dbiterr\_axis ( )

);

endmodule

`default\_nettype wire

Последовательность событий транзакции чтения можно представить следующим образом: ARVALID→ ARREADY→ RVALID→ RREADY.

На рисунке 6 представлена диаграмма чтения данных.

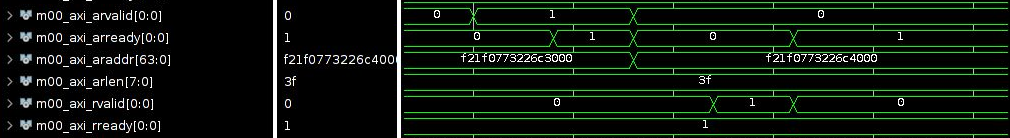


Рисунок 6. Транзакция чтения

Последовательность событий транзакции записи: AWVALID→ AWREADY → WVALID → WREADY → BVALID → BREADY.

На рисунке 7 представлена диаграмма записи данных.

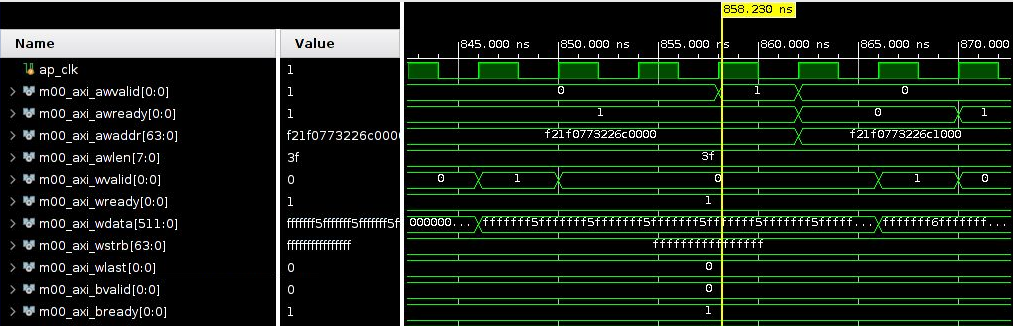


Рисунок 7. Транзакция записи

На рисунке 8 представлена диаграмма инкремента данных в модуле rtl\_kernel\_wizard\_0\_adder.v

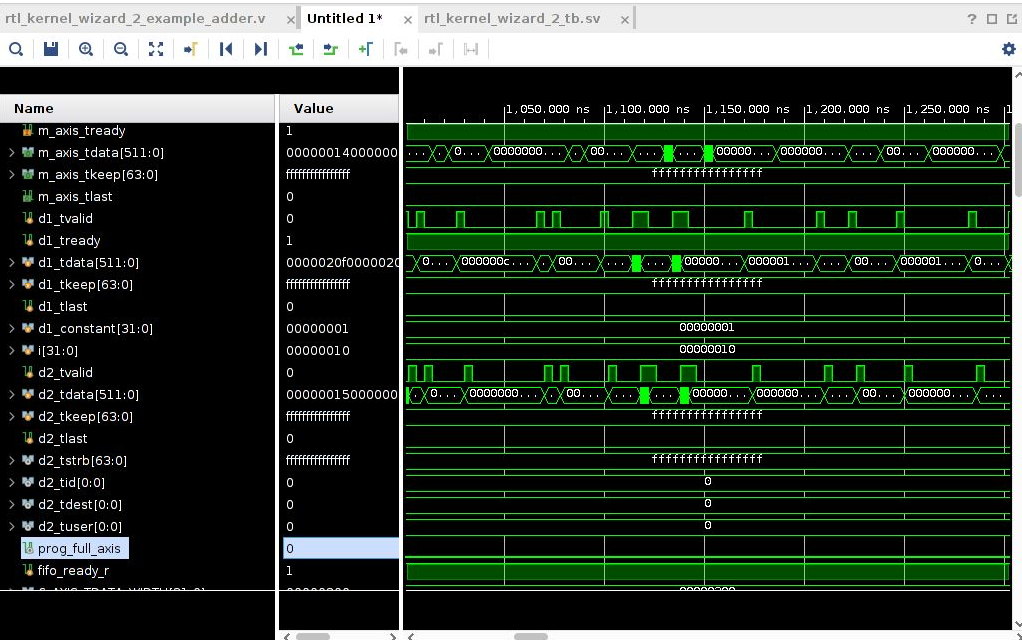


Рисунок 8. Диаграмма «adder’а»

В файле host\_example.cpp были изменена часть кода с проверкой считанного результата операции:

for (cl\_uint i = 0; i < number\_of\_words; i++) {

if **((h\_data[i] / 16 - 11) != h\_axi00\_ptr0\_output[i])** {

printf("ERROR in rtl\_kernel\_wizard\_1::m00\_axi - array index %d (host addr 0x%03x) - input=%d (0x%x), output=%d (0x%x)\n", i, i\*4, h\_data[i], h\_data[i], h\_axi00\_ptr0\_output[i], h\_axi00\_ptr0\_output[i]);

check\_status = 1;

}

// printf("i=%d, input=%d, output=%d\n", i, h\_axi00\_ptr0\_input[i], h\_axi00\_ptr0\_output[i]);

}

На рисунке 9 представлен результат проверки работоспособности программы.

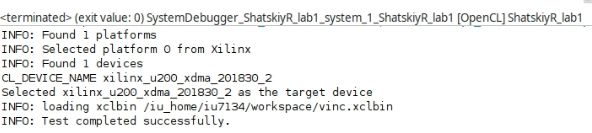


Рисунок 9. Результат проверки

# Контрольные вопросы

1. Назовите преимущества и недостатки XDMA и QDMA платформ.

Сборка QDMA (Queue Direct Memory Access), доступная на картах ускорителей Alveo, предоставляет разработчикам прямое потоковое соединение с низкой задержкой между хостом и ядрами. Оболочка QDMA включает высокопроизводительный DMA, который использует несколько очередей, оптимизированных как для передачи данных с высокой пропускной способностью, так и для передачи данных с большим количеством пакетов. Только QDMA позволяет передавать поток данных непосредственно в логику FPGA параллельно с их обработкой.

Оболочка XDMA требует, чтобы данные сначала были полностью перемещены из памяти хоста в память FPGA (DDRx4 DIMM или PLRAM), прежде чем логика FPGA сможет начать обработку данных, что влияет на задержку на зап уска задачи.

Потоковая передача напрямую в работающие ускорительные ядра (так называемый Free-Running-Mode) позволяет быстро и без излишней буферизации передавать операнды и результаты вычислений на хост по потоковому интерфейсу AXI4 Stream. Решение QDMA подходит для приложений, в которых вычисления строятся на передачи сравнительно небольших пакетов, но при этом требуется высокая производительность и минимальная задержка отклика.

QDMA подходит для потоковой передачи небольших данных, а в остальных случаях больше подходит XDMA.

1. Назовите последовательность действий, необходимых для инициализации ускорителя со стороны хост-системы.

* Получить название целевого ускорителя;
* Получить список всех доступных платформ;
* Выбрать вендора ускорителя (Xilinx);
* Получить список доступных вычислительных устройств;
* Выбрать целевого ускорителя.

1. Какова процедура запуска задания на исполнения в ускорительном ядре VINC.

* Инициализация ускорителя;
* Создание вычислительного контекста целевого ускорителя;
* Создание очереди команд к ускорителю;
* Загрузка слинкованного из объектных файлов ядра бинарного файла в оперативную память (\*.xclbin).
* Создание программы на основе загруженного бинарного файла.
* Настройка маппинга оперативной памяти на входы ядра.
* Запуск задания для ядра на подготовленных входных данных.
* Считывание выходных данных из устройства для проверки корректности работы ядра.
* Освобождение захваченных хост-программой ресурсов.

1. Опишите процесс линковки на основании содержимого файла v++\_\*.log.

* SYSTEM\_LINK
* CFGEN
* CF2BD
* Synthesis (block-level, top-level)
* FPGA linking synthesized kernels to platform
* FPGA logic optimization
* FPGA logic placement
* FPGA routing
* FPGA bitstream generation
* rtdgen
* xclbinutil
* xclbinutilinfo

# Заключение

В ходе работы была изучена архитектура гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx.